What is claimed is:

1. A semiconductor memory array, comprising:

a plurality of semiconductor dynamic random access memory cells arranged in a matrix of rows and columns, each semiconductor dynamic random access memory cell includes at least one transistor having:

a source region;

a drain region;

a body region disposed between and adjacent to the source region and the drain region, wherein the body region is electrically floating; and

a gate spaced apart from, and capacitively coupled to, the body region;

wherein each transistor includes a first state representative of a first charge in the body region, and a second data state representative of a second charge in the body region; and

wherein each row of semiconductor dynamic random access memory cells includes an associated source line which is connected to only the semiconductor dynamic random access memory cells of the associated row.

2. The semiconductor memory array of claim 1 wherein each memory cell of each row of semiconductor dynamic random access memory cells includes a separate bit line which is connected to the drain region of the associated transistor.

3. The semiconductor memory array of claim 2 wherein each memory cell of a first row is programmed to a first data state by applying a control signal, having a first

amplitude, to the gate of the transistor of each memory cell of the first row and a control signal, having a second amplitude, to the drain of each memory cell of the first row.

4. The semiconductor memory array of claim 3 wherein a predetermined memory cell of the first row is programmed to a second data state by applying a control signal, having a third amplitude, to the gate of the transistor of the predetermined memory cell, a control signal, having an fourth amplitude, to the drain of predetermined memory cell, and a control signal, having a fifth amplitude, to the source of predetermined memory cell of the row.

5. The semiconductor memory array of claim 4 wherein an unselected memory cell of the first row is maintained in the first data state, while the predetermined memory cell is programmed to a second data state, by applying a control signal, having a third amplitude, to the gate of the transistor of the predetermined memory cell and a control signal, having an sixth amplitude, to the drain of predetermined memory cell.

6. The semiconductor memory array of claim 5 wherein all of the memory cells of the first row are read by applying a control signal, having a seventh amplitude, to the gate of the transistor of the predetermined memory cell and a control signal, having an eight amplitude, to the drain of predetermined memory cell.

7. The semiconductor memory array of claim 6 wherein all of the memory cells of a second row are maintained in an inhibit state while the memory cells of the first row are read.

8. The semiconductor memory array of claim 6 wherein all of the memory cells of a second row are maintained in an inhibit state while the memory cells of the first row are read by applying a control signal having a ninth amplitude to the gate of the transistors of the memory cells of the second row.

9. The semiconductor memory array of claim 1 wherein each memory cell of a first row of semiconductor dynamic random access memory cells shares a drain region with a memory cell in a second row of semiconductor dynamic random access memory cells, wherein the first and second rows of memory cells are adjacent rows.

10. The semiconductor memory array of claim 1 wherein each gate of each memory cell of a first row of semiconductor dynamic random access memory cells is connected to a first gate line.

11. The semiconductor memory array of claim 1 wherein only the gate of each memory cell of the first row of semiconductor dynamic random access memory cells is connected to the first gate line.

12. A semiconductor memory array, comprising:

a plurality of semiconductor dynamic random access memory cells arranged in a matrix of rows and columns, each semiconductor dynamic random access memory cell includes at least one transistor having:

a source region;

a drain region;

a body region disposed between and adjacent to the source region and the drain region, wherein the body region is electrically floating; and

a gate spaced apart from, and capacitively coupled to, the body region;

wherein each transistor includes a first state representative of a first charge in the body region, and a second data state representative of a second charge in the body region;

wherein each row of semiconductor dynamic random access memory cells includes (1) an associated source line which is connected to only the semiconductor dynamic random access memory cells in the associated row and (2) a different gate line for each semiconductor dynamic random access memory cells in the associated row.

13. The semiconductor memory array of claim 12 wherein each memory cell of each row of semiconductor dynamic random access memory cells includes a separate bit line which is connected to the drain region of the associated transistor.

14. The semiconductor memory array of claim 13 wherein each memory cell of a first row is programmed to a first data state by applying a control signal, having a first

amplitude, to the gate of the transistor of each memory cell of the first row and a control signal, having a second amplitude, to the drain of each memory cell of the first row.

15. The semiconductor memory array of claim 14 wherein a predetermined memory cell of the first row is programmed to a second data state by applying a control signal, having a third amplitude, to the gate of the transistor of the predetermined memory cell, a control signal, having an fourth amplitude, to the drain of predetermined memory cell, and a control signal, having a fifth amplitude, to the source of predetermined memory cell of the row.

16. The semiconductor memory array of claim 15 wherein an unselected memory cell of the first row is maintained in the first data state, while the predetermined memory cell is programmed to a second data state, by applying a control signal, having a third amplitude, to the gate of the transistor of the predetermined memory cell and a control signal, having an sixth amplitude, to the drain of predetermined memory cell.

17. The semiconductor memory array of claim 16 wherein all of the memory cells of the first row are read by applying a control signal, having a seventh amplitude, to the gate of the transistor of the predetermined memory cell and a control signal, having an eight amplitude, to the drain of predetermined memory cell.

18. The semiconductor memory array of claim 17 wherein all of the memory cells of a second row are maintained in an inhibit state while the memory cells of the first row are read.

19. The semiconductor memory array of claim 17 wherein all of the memory cells of a second row are maintained in an inhibit state while the memory cells of the first row are read by applying a control signal having a ninth amplitude to the gate of the transistors of the memory cells of the second row.

20. The semiconductor memory array of claim 12 wherein each memory cell of a first row of semiconductor dynamic random access memory cells shares a drain region with a memory cell in a second row of semiconductor dynamic random access memory cells, wherein the first and second rows of memory cells are adjacent rows.